GZ hdc hidgn

1 SP1000A

1 SP1000A

SP1000A

CPU CPU CPU

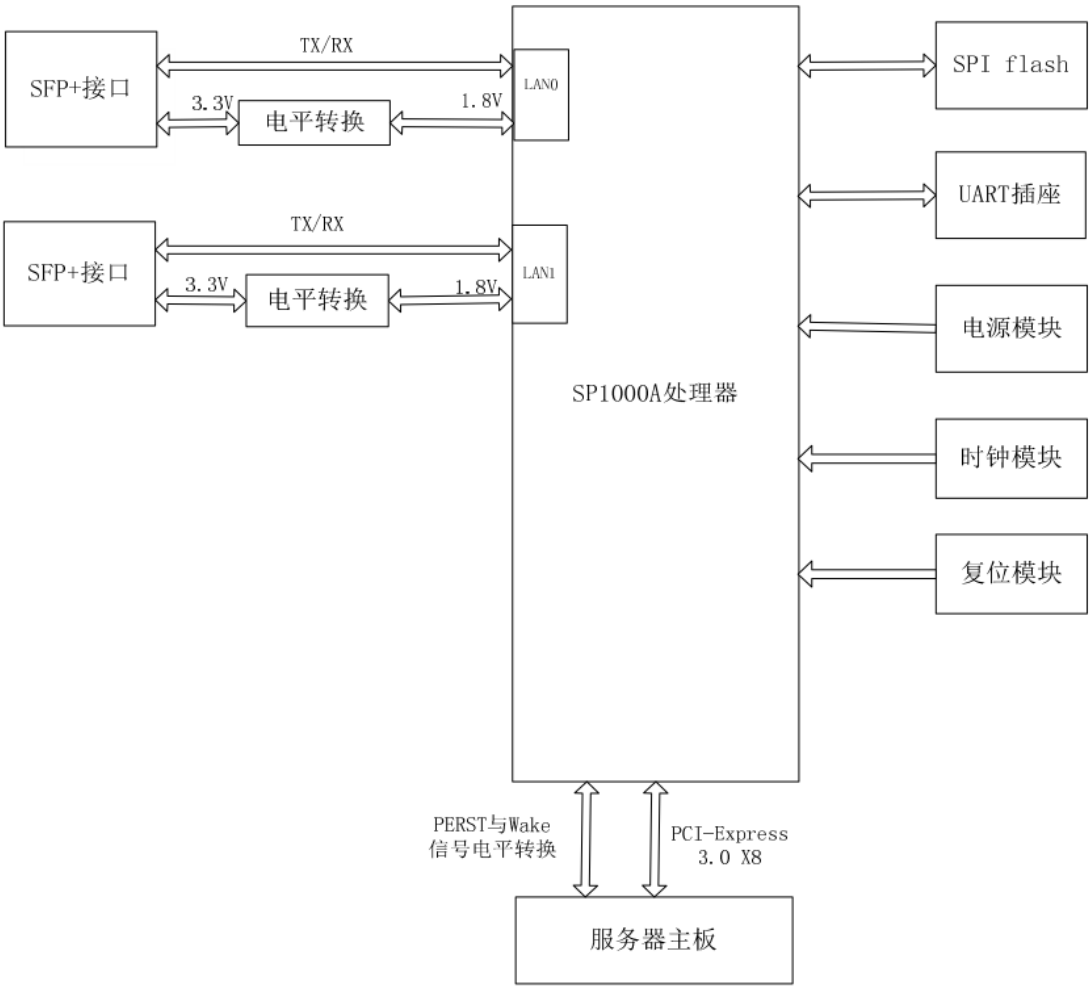
SP1000A 300

PCI Express X8

I/O

SP1000A MAC SFP+

SP1000A



1.1

1.1.1

- 10G SFI/KR/XAUI/SGMII
- 9.5 KB
- 73
- / FIFO
- 802.1q VLAN
-
-

1.1.2

- PFC(802.1Qbb)
- ETS(802.1Qaz)
- QCN(802.1Qau)
- VEPA
- ETAG
- MIB RMON
- VXLAN/Geneve/NVGRE

1.1.3

- IPv4 TCP RSC
- FCOE
- TCP 256KB
- Linksec
- IPSec
- IP/TCP/UDP/STCP
- UDP
- CRC
- VLAN Tag
- MAC / VLAN
-

1.1.4

- MSI / MSI-X
-
- TCP
- TPH/FLR/IDO/ARI/VPD/ECRC
- 256B / 2KB
- PCIE
- D0 D3 ACPI

1.1.5

- SR-IOV
- 128
  - 32
  - 2
- 128
  - LLI
- 64 64 x 2
  63
  - 128 MAC
  - 4096
  - 4096
-

1.1.6

- 10 Gb
- PCIe Gen3 ———x1 x2 x4 x8
- LAN 8 GPIO
- LAN 1 IIC
- SPI
- UART
- NCSI
- 8 GPIO
- SMbus
-

1.2

Note: the single-ended signal IO level standard of SP1000A chip is 1.8V LVCMOS standard.

Table1:Chip status

Ball #	Pin Name	Type	Description
H5	PCIE_BSY	Output	Asserted when PCI Express link has traffic
B1	ETH_UP_1	Active-High	Asserted when Ethernet port1 is UP
C1	ETH_1G_0		Asserted when Ethernet port0 is at 1Gbps
D1	ETH_100M_0		Asserted when Ethernet port0 is at 100Mbps

Ball #	Pin Name	Type	Description
H3	PCIE_PHY_PARA_SEL		Active-High. If asserted, PHY Internal registers are accessed by Internal logic, otherwise PHY Internal registers are accessed by JTAG.
H1	ETH_PHY_PARA_SEL		
G1	ETH_PHY_SRAM_BYPASS		Active-High. If asserted, PHY Internal SRAM is bypassed.

Table4:Ethernet Port1 PHY

Ball #	Pin Name	Type	Description
A18	ETH1_RX_N_0	Input	CML differential signal, Ethernet Port1 PHY differential pairs, ETH1_RX_0 differential pair for connection to SFI RX, ETH1_TX_0 differential pair for connection to SFI TX.

Ball #	Pin Name	Type	Description
AB10	PE_RX_N_3	Input	
V12	PE_TX_P_4	Output	
W12	PE_TX_N_4	Output	
AA12	PE_RX_P_4	Input	
AB12	PE_RX_N_4	Input	
V14	PE_TX_P_5	Output	
W14	PE_TX_N_5	Output	
AA14	PE_RX_P_5	Input	
AB14	PE_RX_N_5	Input	
V16	PE_TX_P_6	Output	
W16	PE_TX_N_6	Output	
AA16	PE_RX_P_6	Input	
AB16	PE_RX_N_6	Input	
V18	PE_TX_P_7	Output	
W18	PE_TX_N_7	Output	
AA18	PE_RX_P_7	Input	
AB18	PE_RX_N_7	Input	

Table6:SPI Flash

Ball #	Pin Name	Type	Description
E20	SPI_CLK_DIV_0	Input	They create a 3-bit bus. Its value determines the SPI clock (250MHz/X, where X is determined by these three signals): 1. □ MHz 2. □ 3. □ 4. □ 5. □ 6. □ 7. □
D22	SPI_CLK_DIV_1		
D21	SPI_CLK_DIV_2		□
B20	SPI_CLK	Output	SPI Interface from SP to Flash
C20	SPI_SO	Output	
C21	SPI_SI	Input	
C22	SPI_CS_N	Output	

Table7:UART

Ball #	Pin Name	Type	Description
J2	UART_STX	Output	UART Interface to on-chip CPU

Ball #	Pin Name	Type	Description
J3	UART_SRX	Input	

Table8:Ethernet GPIO

Ball #	Pin Name	Type	Description
M3	LAN0_GPIO_0	BiDir	LAN0/1 GPIO. They are used to get status of optical module, LAN GPIO design related to network card driver.
M4	LAN0_GPIO_1		
N3	LAN0_GPIO_2		
N1	LAN0_GPIO_3		
N2	LAN0_GPIO_4		
P3	LAN0_GPIO_5		
N5	LAN0_GPIO_6		
P1	LAN0_GPIO_7		
P4	LAN1_GPIO_0		
P5	LAN1_GPIO_1		
R4	LAN1_GPIO_2		
R2	LAN1_GPIO_3		
R3	LAN1_GPIO_4		
T2	LAN1_GPIO_5		
R5	LAN1_GPIO_6		
T1	LAN1_GPIO_7		

Table9:MNG GPIO

Ball #	Pin Name	Type	Description
R21	MNG_GPIO_0	BiDir	Universal input and output pin of internal embedded CPU, if not used can be left unconnected.
R19	MNG_GPIO_1		
P18	MNG_GPIO_2		
P19	MNG_GPIO_3		
R22	MNG_GPIO_4		
P22	MNG_GPIO_5		
N18	MNG_GPIO_6		
P20	MNG_GPIO_7		

Table10:NCSI

Ball #	Pin Name	Type	Description
T22	RMII_TXD_0	Output	NCSI transmit data
R18	RMII_TXD_1		
U20	RMII_TX_EN	Output	Transmit Enable
V21	RMII_CSR_DV	Input	Carrier Sense/Receive Data Valid
V22	RMII_REF_CLK	Input	NCSI reference clock

Ball #	Pin Name	Type	Description
U22	RMII_RXD_0	Input	NCSI receive data
T20	RMII_RXD_1		

Table11:MII

Ball #	Pin Name	Type	Description
R20	MII_MD	BiDir	If NCSI is connected to PHY, this Interface is used to control the PHY, otherwise it is not connected by default.
T21	MII_MDC	Output	

Table12:IIC

Ball #	Pin Name	Type	Description
F2	IIC0_SCL	BiDir	I2C Interface for laser module configuration Input 10G PHY
F3	IIC0_SDA		
G3	IIC1_SDA		
F1	IIC1_SCL		

Table13:MDIO

Ball #	Pin Name	Type	Description
U1	MD1_CLK	Output	Used to control external PHY if SP is using external PHY.
V2	MD1_IO	BiDir	
U3	MD0_CLK	Output	
T3	MD0_IO	BiDir	

Table14:MNG SMBus

Ball #	Pin Name	Type	Description
J1	MNG_IC_DATA	OD	SMBus to on-chip CPU
K1	MNG_IC_SMBALERT_N	Output	
K3	MNG_IC_SMBSUS_N	Output	
K5	MNG_IC_CLK	OD	

Table15:Probe

Ball #	Pin Name	Type	Description
E22	PRB_EN	Input	Testing signals. They are not used Input normal operations.
D20	PRB_HIT	Output	
N21	PRB_CLKOUTPUT		
N22	PRB_DATA_0		

Ball #	Pin Name	Type	Description
N20	PRB_DATA_1		
M19	PRB_DATA_2		
M20	PRB_DATA_3		
M18	PRB_DATA_4		
M22	PRB_DATA_5		
L18	PRB_DATA_6		
M21	PRB_DATA_7		
L20	PRB_DATA_8		
L22	PRB_DATA_9		
L19	PRB_DATA_10		
K21	PRB_DATA_11		
K22	PRB_DATA_12		
K20	PRB_DATA_13		
J22	PRB_DATA_14		
K18	PRB_DATA_15		
J21	PRB_DATA_16		
J19	PRB_DATA_17		
J20	PRB_DATA_18		
J18	PRB_DATA_19		
H20	PRB_DATA_20		
H22	PRB_DATA_21		
H19	PRB_DATA_22		
G22	PRB_DATA_23		
H18	PRB_DATA_24		
G21	PRB_DATA_25		
G18	PRB_DATA_26		
G20	PRB_DATA_27		
F22	PRB_DATA_28		
F20	PRB_DATA_29		
F21	PRB_DATA_30		
F19	PRB_DATA_31		

Table16:JTAG

Ball #	Pin Name	Type	Description
W20	JTAG_SEL_0	Input	JTAG signals for testing purpose. They are not used Input normal operations.
W21	JTAG_SEL_1	Input	
Y20	JTAG_SEL_2	Input	
Y22	JTRST_N	Input	
W22	JTDO	Output	
U19	JTMS	Input	
V20	JTDI	Input	

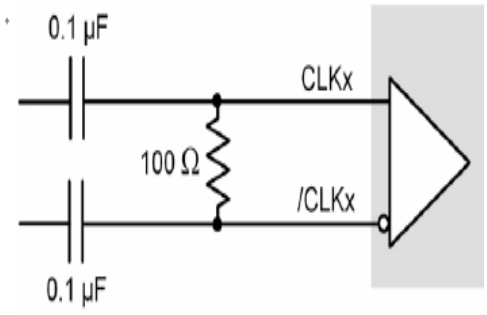
Ball #	Pin Name	Description
M12 P12 N13 M14 P14 N15		that can be shutdown Input low power state.
J8	VSS_A_0P9	Ground for analog 0.9V
J6 K6 L6 M6 N6 P6 J17 K17 L17 M17 N17 P17	VSS_D_1P8	Ground for digital 1.8V
J7 K7 L7 M7 N7 P7 J16 K16 L16 M16 N16 P16	VDD_D_1P8	Power supply for digital 1.8V
H8	VDD_A_1P8	Power supply for analog 1.8V
H9 H10 F11 G11 H11 G12 H12 H13 H14 H15	VP_ETH_A_0P9	Power supply for analog 0.9V used by Ethernet PHY.
G6 G7 G15 G16	VPH_ETH_A_1P8	Power supply for analog 1.8V used by Ethernet PHY.
R8 T8 R9 T9 R10 R12 R13 T13 R14 T14	VP_PE_A_0P9	Power supply for analog 0.9V used by PCI Express PHY.
T6 T7 T15 T16	VPH_PE_A_1P8	Power supply for analog 1.8V used by PCI Express PHY.
H6	TEMPSENSOR_VSSA	1.8V Ground dedicated for temperature sensor
H7	TEMPSENSOR_VDDA	1.8V Power supply dedicated for temperature sensor.

1.3

1.3.1

SP1000A	TEST_MODE_0	TEST_MODE_1	TEST_MODE_2

ETH0_REF_CLK_P ETH0_REF_CLK_N ETH1_REF_CLK_P ETH1_REF_CLK_N
100 1% AC



1.3.6

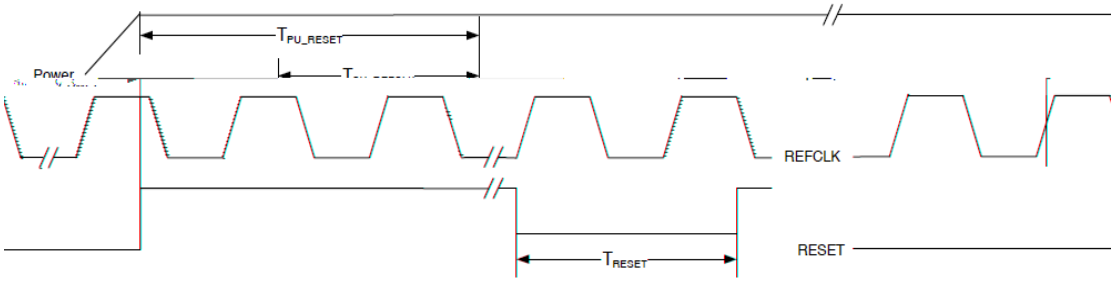
SP1000A 0.9V 1.8V PHY
VP_PE\VP_ETH 0.9V VPH\VDDA18 1.8V
BLM21PG300SN1 10nF\100nF\4.7uF\10
uF\47 uF 0.9V 8A 1.8V
1.5A 5W

1.3.7

SP1000A

TPU_RESET(RESET)	10			ms
TRESET	10			ms

Table21



1.3.8 NCSI AC Specification

The SP1000A is designed to support the standard DMTF NCSI interface. For NCSI I/F timing specification see the following table.

Tckf	NCSI_REF_CLK Frequency		50		MHz
Rdc	NCSI_REF_CLK duty cycle	35		65	%
Racc	NCSI_REF_CLK accuracy			100	ppm
Tco	Clock-to-out (10 pF =< cload <=50 pF) NCSI_RXD[1:0], NCSI_CSR_DV Data valid from NCSI_REF_CLK rising edge	3		4	ns
Tsu	NCSI_TXD[1:0], NCSI_TX_EN Data Setup to NCSI_CLK_IN rising edge	3			ns
Thold	NCSI_TXD[1:0], NCSI_TX_EN Data hold from NCSI_REF_CLK rising edge	1			ns
Tor	NCSI_RXD[1:0], NCSI_CSR_DV Output Time rise	0.5		6	ns
Tof	NCSI_RXD[1:0], NCSI_CSR_DV Output Time fall	0.5		6	ns
Tckr/Tckf	NCSI_REF_CLK Rise/Fall Time	0.5		3.5	ns

1.3.9 FLASH

l cWdc	L F + L
b XgdX e	HHI +L - 7
V Z XZ	9 AF-

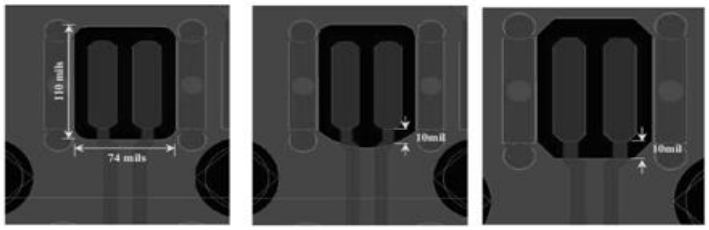
Table22 SPI FLASH

1.3.10

6 V d	6 7G" HBO
ciZa	I AM- 9 78 "I
"idcZ	I 8H"- M" 9mm
c hVg	I AM- 9 78A

Net-

- SFP
- SFI TX RX



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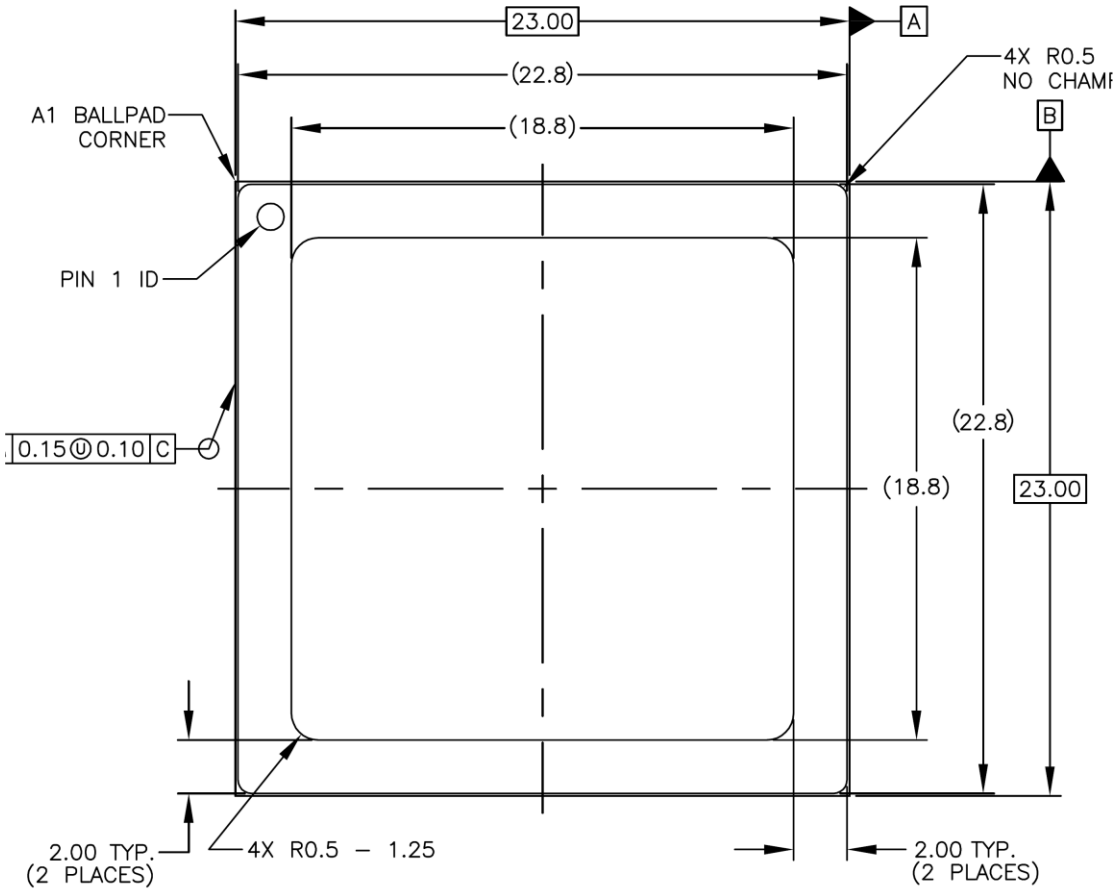
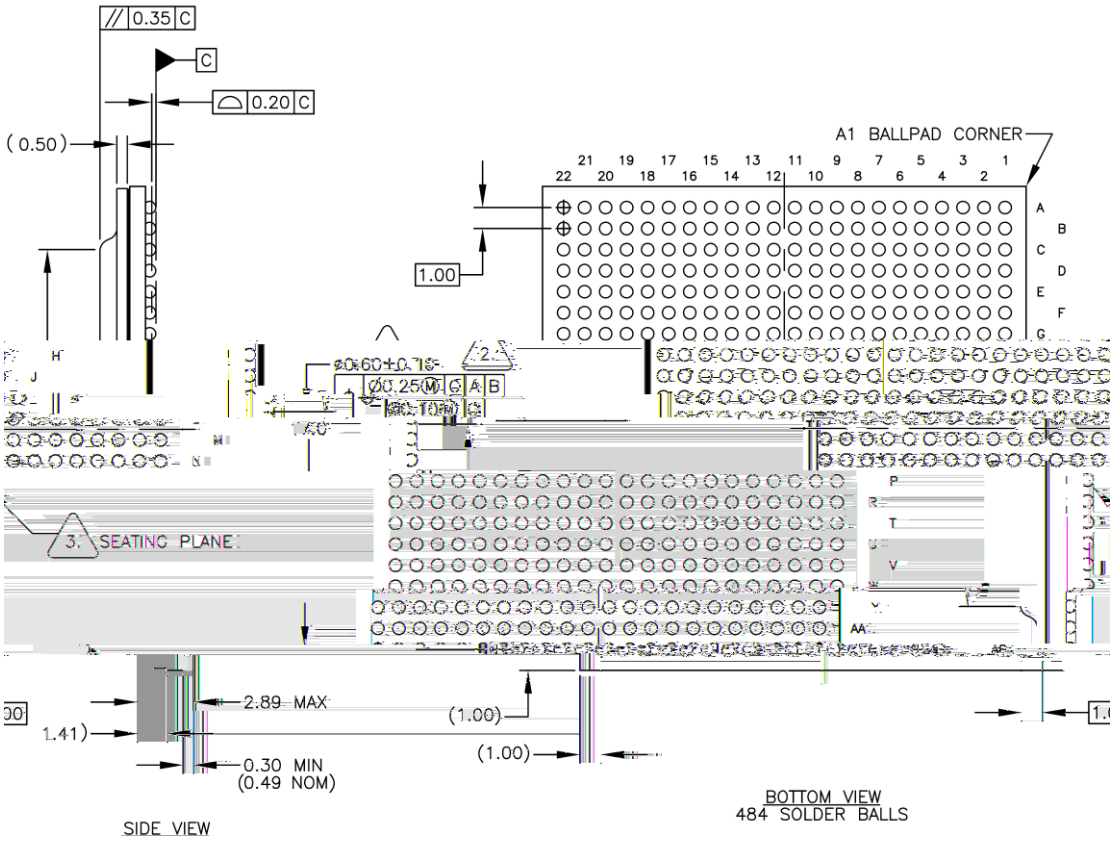


TOP VIEW


0.35 C
C
0.20 C
(0.50)
A1 BALLPAD CORNER
1.00
SEATING PLANE
2.89 MAX
1.41)
0.30 MIN
(0.49 NOM)
(1.00)
(1.00)
SIDE VIEW
BOTTOM VIEW
484 SOLDER BALLS